Notice of Allowability	Application No.	Applicant(s)	
	10/646,957	FRISCH, ARNOLD M.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *08/08/2006*.

2. ☒ The allowed claim(s) is/are *1-35*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/5/2003
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Allowable Subject Matter

1. Claims 1-35 are allowed.

2. Applicant's arguments, filed 08/08/2006, have been fully considered and are persuasive. The rejection of 04/27/2006 has been withdrawn.

3. The following is an examiner's statement of reasons for allowance:

The present invention pertains to integrated jitter generators for adding a controlled amount of jitter to a signal during a jitter test.

The claimed invention in claim 1 recites features such as:"...an apparatus for providing a jittery test signal for use in an integrated circuit (IC) test, the apparatus comprising: a programmable delay circuit for delaying a first signal with an adjustable delay controlled by an input digital delay word to produce the jittery test signal for use in the IC; and first means for supplying a sequence of digital data words as input to the programmable delay circuit for varying the adjustable delay so that the test signal jitters relative to the first signal."

The prior art of record (Dinteman US 5,948,115) teaches that Programmable delay circuit 54 delays the timing signal TD with a delay determined by delay data (DELAY) produced by pattern generator 56, thereby to provide a delayed timing signal TD' to a shift-out (SO) input of FIFO buffer 52. Pattern generator 56 sets the DELAY data value provided to delay circuit 54 after each pulse of timing signal TD in accordance with a pattern defined by programming data provided as input to pattern generator 56 via computer bus 16. In response to each pulse of delayed timing signal TD', FIFO buffer 52 shifts its longest stored control bit onto a data-out terminal (DO) as the DRIVE signal provided to drive circuit 40 of FIG. 4 (fig. 4, 6, col. 6, lines 39-51, Dinteman).

However Dinteman does not teach an apparatus for providing a jittery test signal for use in an integrated circuit (IC) test, the apparatus comprising: a programmable delay circuit for delaying a first signal with an adjustable delay controlled by an input digital delay word to produce the jittery test signal for use in the IC; and first means for supplying a sequence of digital data words as input to the programmable delay circuit for varying the adjustable delay so that the test signal jitters relative to the first signal.

Hence, the prior arts of record do not anticipate nor render obvious the claimed invention. Thus, claim 1 is allowable over the prior arts of record. Claims 2-21 are allowed because of the combination of additional limitations and the limitations listed above.

- The claimed invention in claim 22 recites features such as:"...a method for testing a subcircuit of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal, the method comprising the steps of: a. providing a programmable delay circuit having an adjustable delay controlled by digital delay control data supplied to the programmable delay control circuit; b. applying a first signal as input to the programmable delay circuit such that the programmable delay circuit delays the first signal to produce a test signal, and c. supplying a sequence of digital control data to the programmable delay circuit that varies the adjustable delay during step b such that the test signal jitters relative to the first signal."

The prior art of record (Dinteman US 5,948,115) teaches that Programmable delay circuit 54 delays the timing signal TD with a delay determined by delay data (DELAY) produced by pattern generator 56, thereby to provide a delayed timing signal TD' to a shift-out (SO) input of FIFO buffer 52. Pattern generator 56 sets the DELAY data value provided to delay circuit 54 after each pulse of timing signal TD in accordance with a pattern defined by programming data provided as input to pattern generator 56 via computer bus 16. In response to each pulse of delayed timing signal TD', FIFO buffer 52 shifts its longest stored control bit onto a data-out terminal (DO) as the DRIVE signal provided to drive circuit 40 of FIG. 4 (fig. 4, 6, col. 6, lines 39-51, Dinteman).

Bhawmik et al. (US 6,463,560 B1) teach that testing of the IC may be accomplished by applying a test pattern to stimulate the inputs of a circuit and monitoring the output response to detect the occurrence of faults. The pattern generator may be a BIST structure (col. 1, lines 16-22, Bhawmik et al.).

Neither Dinteman nor Bhawmik et al. teach a method for testing a subcircuit of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal, the method comprising the steps of: a. providing a programmable delay circuit having an adjustable delay controlled by digital delay control data supplied to the programmable delay control circuit; b. applying a first signal as input to the programmable delay circuit such that the programmable delay circuit delays the

first signal to produce a test signal, and c. supplying a sequence of digital control data to the programmable delay circuit that varies the adjustable delay during step b such that the test signal jitters relative to the first signal.

Hence, the prior arts of record do not anticipate nor render obvious the claimed invention. Thus, claim 22 is allowable over the prior arts of record. Claims 23-30 are allowed because of the combination of additional limitations and the limitations listed above.

- The claimed invention in claim 31 recites features such as:"...an apparatus for testing a subcircuit of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal, the apparatus comprising: a programmable delay circuit residing within the IC for delaying a first clock signal to with a delay selected by a digital delay control word input to the programmable delay circuit to produce a second clock signal; a programmable pattern generator for providing a sequence of delay control words as input to the programmable delay circuit; first means for selectively applying the second clock signal as the input signal to the subcircuit; a multiplexer residing within the IC for receiving a third clock signal and the second clock signal for selectively supplying either the third clock signal or the second clock signal as the first clock signal input to the programmable delay circuit, wherein the second clock signal oscillates when supplied as the first clock signal input to the programmable delay circuit with a period that is a function of the delay provided by the programmable delay circuit; and a test circuit receiving the second clock signal and for generating a test signal having edges synchronized to edges of the second clock signal."

The prior art of record (Dinteman US 5,948,115) teaches that Programmable delay circuit 54 delays the timing signal TD with a delay determined by delay data (DELAY) produced by pattern generator 56, thereby to provide a delayed timing signal TD' to a shift-out (SO) input of FIFO buffer 52. Pattern generator 56 sets the DELAY data value provided to delay circuit 54 after each pulse of timing signal TD in accordance with a pattern defined by programming data provided as input to pattern generator 56 via computer bus 16. In response to each pulse of delayed timing signal TD', FIFO buffer 52 shifts its longest stored control bit onto a data-out terminal (DO) as the DRIVE signal provided to drive circuit 40 of FIG. 4 (fig. 4, 6, col. 6, lines 39-51, Dinteman).

Bhawmik et al. (US 6,463,560 B1) teach that testing of the IC may be accomplished by applying a test pattern to stimulate the inputs of a circuit and monitoring the output response to detect the occurrence of faults. The pattern generator may be a BIST structure (col. 1, lines 16-22, Bhawmik et al.).

Osawa et al. (US 5,815,512) teach a semiconductor memory testing device (col. 4, lines 64-65, Osawa et al.). Osawa et al. teach the selector circuit to select the signal input terminal "0" in a normal operation and a test mode on the basis of the external shift mode control signal (SM) while selecting the other signal input terminal "1" in shift mode on the basis of the shift mode control signal (col. 33, lines 57-67, Osawa et al.).

Chetlur et al. (US 6,535,014 B2) teach an integrated circuit comprising: a tester for a circuit path including a voltage controlled oscillator (VCO) for generating a controllable frequency oscillating test signal and having a controllable amplitude defined between first and second voltages, a multiplexer for selectively connecting one of the oscillating test signal, the first voltage, and the second voltage to the circuit path, and a selector for selectively connecting the multiplexer to the circuit path (col. 2, lines 4-12, Chetlur et al.). Chetlur et al. also teach that the circuit paths, the VCO, the multiplexer, and the selector may be integrated on a circuit chip (col. 2, lines 18-20, Chetlur et al.).

Speyer et al. (US 6,611,477 B1) teach that a test circuit is provided with a feedback path so that the test circuit and feedback path together form a free-running oscillator (col. 2, lines 48-51, Speyer et al.).

Churchill et al. (US 6,006,347) teach the integrated circuit, wherein the programmable scan circuit comprises: a logic circuit selectively decoding the scan data; and a programmable delay circuit coupled to the logic circuit (col. 20, lines 28-31, Churchill et al.).

However the prior arts of record do not teach an apparatus for testing a subcircuit of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal, the apparatus comprising: a programmable delay circuit residing within the IC for delaying a first clock signal to with a delay selected by a digital delay control word input to the programmable delay circuit to produce a second clock signal; a programmable pattern generator for providing a sequence of delay control words as input to the programmable delay circuit; first means for selectively applying the second clock signal as the input signal to the subcircuit; a multiplexer residing within the IC for receiving

a third clock signal and the second clock signal for selectively supplying either the third clock signal or the second clock signal as the first clock signal input to the programmable delay circuit, wherein the second clock signal oscillates when supplied as the first clock signal input to the programmable delay circuit with a period that is a function of the delay provided by the programmable delay circuit; and a test circuit receiving the second clock signal and for generating a test signal having edges synchronized to edges of the second clock signal.

Hence, the prior arts of record do not anticipate nor render obvious the claimed invention. Thus, claim 31 is allowable over the prior arts of record. Claims 32-35 are allowed because of the combination of additional limitations and the limitations listed above.

- Thus, claims 1-35 are allowable over the prior arts of record,

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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